CMOSTEK CMT2300A

Ultra Low Power Sub-1GHz RF Transceiver

Features:

- Frequency range: 140 ~1020MHz
- Modem: OOK, (G)FSK 和(G)MSK
- Data rate: 0.5 ~ 300 kbps
- Sensitivity: -121 dBm 2.0 kbps, F_{RF} = 433.92 MHz
  -111 dBm 50 kbps, F_{RF} = 433.92 MHz
- Voltage range: 1.8 ~3.6 V
- Transmit current: 23 mA @ 13 dBm, 433.92 MHz, FSK
  72 mA @ 20 dBm, 433.92 MHz, FSK,
- Rx current: 8.5 mA @ 433.92 MHz, FSK (High power mode)
  7.2 mA @ 433.92 MHz, FSK (Low power mode)
- Super Low Power mode
- Sleep current: 300 nA, Duty Cycle = OFF
  800 nA, Duty Cycle = ON
- 4-wire SPI interface
- Direct and packet mode supported
- Configurable packet processor and 64-Byte FIFO.
- NRZ, Manchester codec, Whitening codec.
- Forward Error Correction
- 16 pin QFN3x3 package

Descriptions:

CMT2300A is an ultra low power, high performance, OOK (G) FSK RF transceiver suitable for a variety of 140 to 1020 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ RF product line. The product line contains the complete transmitters, receivers and transceivers. The high integration of CMT2300A simplifies the peripheral materials required in the system design. Up to +20 dBm Tx Power and -121 dBm sensitivity optimize the performance of the application. It supports a variety of packet formats and codec methods. It is flexible to meet the needs of various applications for different packet formats and codec methods. In addition, CMT2300A also supports 64-byte Tx/Rx FIFO,GPIO and interrupt configuration, Duty-Cycle operation mode, channel sensing, high-precision RSSI, low-voltage detection, power-on reset, low frequency clock output, manual Fast Frequency Hopping, squelch and etc. The features make the application design more flexible differentiated. CMT2300A operates from 1.8 V to 3.6 V. Only 8.5 mA current is consumed when the sensitivity is -121 dBm, Super Low Power mode can further reduces the chip power consumption. Only 23 mA Tx current is consumed when the output power is 13dBm.

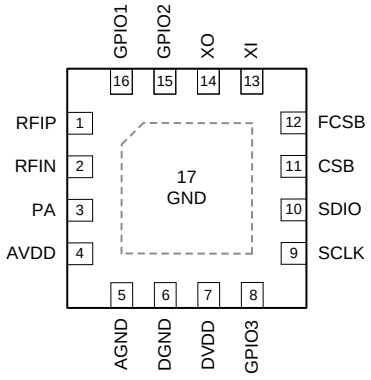
Applications:

- Automatic meter reading
- Home security and building automation
- ISM band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor node
- Tag reader

Ordering information

Model	Frequency	Package	MOQ
CMT2300A-EQR	433.92 MHz	QFN16	5,000 pcs
For more information, see Page 36 Table 29.			

QFN16 (3x3)



CMT2300A top view

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1. Electrical Characteristics

V_{DD}= 3.3 V, T_{OP}= 25 °C, F_{RF} = 433.92 MHz, The sensitivity is measured by receiving a PN9 timing and matching the impedance to 50Ω under the 0.1%BER standard. Unless otherwise stated, all results are tested on the CMT2300A-EM evaluation board.

1.1 Recommended Operation Condition

Table 1. Recommended operation condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Power voltage slope			1			mV/us

1.2 Absolute Maximum Rating

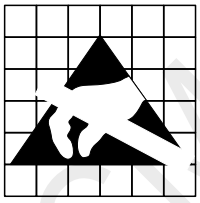
Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating[2]		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Notes:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2].



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Table 3. Power consumption specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep timer is off		300		nA
		Sleep mode, sleep timer is on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator is on		1.45		mA
RFS current	I_{RFS}	433 MHz		5.7		mA
		868 MHz		5.8		mA
		915 MHz		5.8		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
RX current (high power mode)	I_{Rx-HP}	FSK, 433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		FSK, 915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
RX current(low power mode)	I_{Rx-LP}	FSK, 433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		FSK, 915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA
TX current	I_{Tx}	FSK, 433 MHz, +20 dBm (Direct Tie)		72		mA
		FSK, 433 MHz, +20 dBm (RF switch)		77		mA
		FSK, 433 MHz, +13 dBm (Direct Tie)		23		mA
		FSK, 433 MHz, +10 dBm (Direct Tie)		18		mA
		FSK, 433 MHz, -10 dBm(Direct Tie)		8		mA
		FSK, 868 MHz, +20 dBm(Direct Tie)		87		mA
		FSK, 868 MHz, +20 dBm(RF switch)		80		mA
		FSK, 868 MHz, +13 dBm (Direct Tie)		27		mA
		FSK, 868 MHz, +10 dBm (Direct Tie)		19		mA
		FSK, 868 MHz, -10 dBm (Direct Tie)		8		mA
		FSK, 915 MHz, +20 dBm (Direct Tie)		70		mA
		FSK, 915 MHz, +20 dBm (RF switch)		75		mA
		FSK, 915 MHz, +13 dBm (Direct Tie)		28		mA
		FSK, 915 MHz, +10 dBm (Direct Tie)		19		mA
		FSK, 915 MHz, -10 dBm (Direct Tie)		8		mA

1.4 Receiver

Table 4. Receiver specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR	OOK	0.5		40	kbps
		FSK and GFSK	0.5		300	kbps
Deviation	F_{DEV}	FSK and GFSK	2		200	kHz
Sensitivity @ 433 MHz	$S_{433\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power setting）		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--103		dBm
Sensitivity @ 868 MHz	$S_{868\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power setting）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity @ 915 MHz	$S_{915\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-117		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power mode）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power mode）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--99		dBm
Saturation Input Signal Level	P_{LVL}				20	dBm
Image Rejection Ratio	IMR	F_{RF}=433 MHz		35		dBc
		F_{RF}=868 MHz		33		dBc
		F_{RF}=915 MHz		33		dBc
RX Channel Bandwidth	BW	RX channel bandwidth	50		500	kHz
Co-channel Rejection Ratio	CCR	DR = 10 kbps, F_{DEV} = 10 kHz; Interference with the same modulation		-7		dBc

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Adjacent Channel Rejection Ratio	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 200 kHz Channel spacing, interference with the same modulation		30		dBc
Alternate Channel Rejection Ratio	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 400 kHz Channel spacing, interference with the same modulation		45		dBc
Blocking Rejection Ratio	BI	DR = 10 kbps, F_{DEV} = 10 kHz; ±1 MHz Deviation, continuous wave interference		70		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ± 2 MHz Deviation, continuous wave interference		72		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ±10 MHz Deviation, continuous wave interference		75		dBc
Input 3rd Order Intercept Point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz; 1 MHz and 2 MHz Deviation dual tone test, maximum system gain setting.		-25		dBm
RSSI Range	RSSI		-120		20	dBm

1.5 Transmitter

Table 5. Transmitter specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Need specific peripheral materials for different frequency bands	-20		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Output power variation	$P_{OUT-TOP}$	Temperature from -40 to +85 °C		1		dB
Stray radiation		P_{OUT} = +13 dBm,433MHz, F_{RF}<1 GHz			-42	dBm
		1 GHz to 12.75 GHz, with harmonic			-36	dBm
Harmonic output for F_{RF}= 433 MHz[1]	$H2_{433}$	2nd harmonic +20 dBm P_{OUT}		-46		dBm
	$H3_{433}$	3nd harmonic +20 dBm P_{OUT}		-50		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2nd harmonic +20 dBm P_{OUT}		-43		dBm
	$H3_{868}$	3nd harmonic +20 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{868}$	2nd harmonic +20 dBm P_{OUT}		-48		dBm
	$H3_{868}$	3nd harmonic +20 dBm P_{OUT}		-53		dBm
Harmonic output for F_{RF}= 433 MHz[1]	$H2_{433}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{433}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{868}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm

1.6 Settle Time

Table 6. Settle Time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settle time	T_{SLP-RX}	From Sleep to RX		1000		us
	T_{SLP-TX}	From Sleep to TX		1000		us
	T_{STB-RX}	From Standby to RX		300		us
	T_{STB-TX}	From Standby to TX		300		us
	T_{RFS-RX}	From RFS to RX		10		us
	T_{TFS-RX}	From TFS to TX		10		us
	T_{TX-RX}	From TX to RX （Ramp Down time needs $2T_{symbol}$ ）		$2T_{symbol}$ +300		us
	T_{RX-TX}	From RX to TX		300		us

1.7 Frequency Synthesizer

Table 7. Frequency Synthesizer Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Need different matching networks	840		1020	MHz
			420		510	MHz
			280		340	MHz
			210		255	MHz
			140		170	MHz
Frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise@ 433 MHz	PN_{433}	10 kHz frequency deviation		-94		dBc/Hz
		100 kHz frequency deviation		-99		dBc/Hz
		500 kHz frequency deviation		-118		dBc/Hz
		1MHz frequency deviation		-127		dBc/Hz
		10 MHz frequency deviation		-134		dBc/Hz
Phase noise@ 868 MHz	PN_{868}	10 kHz frequency deviation		-92		dBc/Hz
		100 kHz frequency deviation		95		dBc/Hz
		500 kHz frequency deviation		-114		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz frequency deviation		-89		dBc/Hz
		100 kHz frequency deviation		-92		dBc/Hz
		500 kHz frequency deviation		-111		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz

1.8 Crystal Oscillator

Table 8. Crystal Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Equivalent resistance	Rm			60		Ω
Start-up time[3]	t_{XTAL}			400		us

Remarks:

[1]. CMT2300A can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3V and 0.7V.

[2]. The value includes (1) initial error; (2) crystal load; (3) aging; and (4) change with temperature. The acceptable crystal frequency tolerance is limited by the receiver bandwidth and the RF frequency offset between the transmitter and the receiver.

[3]. The parameter is largely related to the crystal.

1.9 Low Frequency Oscillator

Table 9. Low Frequency Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Calibration frequency [1]	F_{LPOSC}			32		kHz
Frequency accuracy		After calibration		1		%
Temperature coefficient [2]				-0.02		%/°C
Supply voltage coefficient [3]				+0.5		%/V
Initial calibration time	$t_{LPOSC-CAL}$			4		ms

Remarks:

[1]. The low frequency oscillator is automatically calibrated to the crystal oscillator frequency at the PUP stage and periodically calibrated at this stage.

[2]. After calibration, the frequency changes with temperature.

[3]. After calibration, the frequency changes with the change of the supply voltage.

1.10 Low Battery Detection

Table 10. Low Battery detection specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection accuracy	LBD_{RES}			50		mV

1.11 Digital Interface

Table 11. Digital interface specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input high level	V_{IH}		0.8			V_{DD}
Digital input low level	V_{IL}				0.2	V_{DD}
Digital output high level	V_{OH}	@I_{OH}= -0.5mA	Vdd-0.4			V
Digital output low level	V_{OL}	@I_{OL}= 0.5mA			0.4	V
SCL Frequency	F_{SCL}				5	MHz
SCL high time	T_{CH}		50			ns
SCL low time	T_{CL}		50			ns
SCL rise time	T_{CR}		50			ns
SCL fall time	T_{CF}		50			ns

2. Pin Descriptions

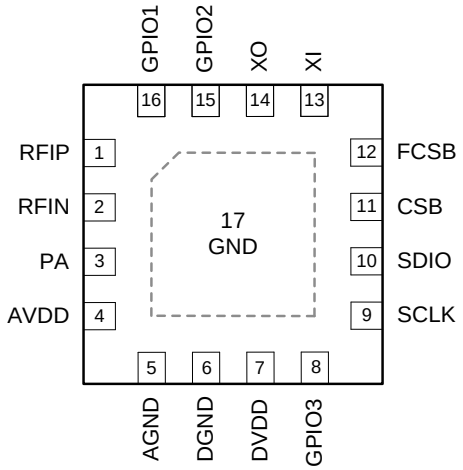


Figure 1. CMT2300A pin arrangements

Table 12. CMT2300A pin descriptions

Pin No.	Name	I/O	Descriptions
1	RFIP	I	RF signal input P
2	RFIN	I	RF signal input N
3	PA	O	PA output
4	AVDD	IO	Analog VDD
5	AGND	IO	Analog GND
6	DGND	IO	Digital GND
7	DVDD	IO	Digital VDD
8[1]	GPIO3	IO	Configured as CLKO, DOUT/DIN, INT2 and DCLK (TX/RX)
9	SCLK	I	SPI clock
10	SDIO	IO	SPI data input and output
11	CSB	I	SPI chip selection bar for register access, active low
12	FCSB	I	SPI chip selection bar for FIFO access ,active low
13	XI	I	Crystal circuit input
14	XO	O	Crystal circuit output
15[1]	GPIO2	IO	Configured as INT1, INT2, DOUT/DIN, DCLK (TX/RX) and RF_SWT
16[1]	GPIO1	IO	Configured as DOUT/DIN, INT1, INT2, DCLK (TX/RX) and RF_SWT
17	GND	I	Analog GND. It must be grounded.

Note:

[1]. INT1 and INT2 are interrupts. DOUT is demodulated output. DIN is a modulation input. DCLK is a modulation or demodulation data rate synchronization clock, automatic switching in TX/RX mode.

3. Typical Application Schematic

3.1 Direct tie Schematic Diagram

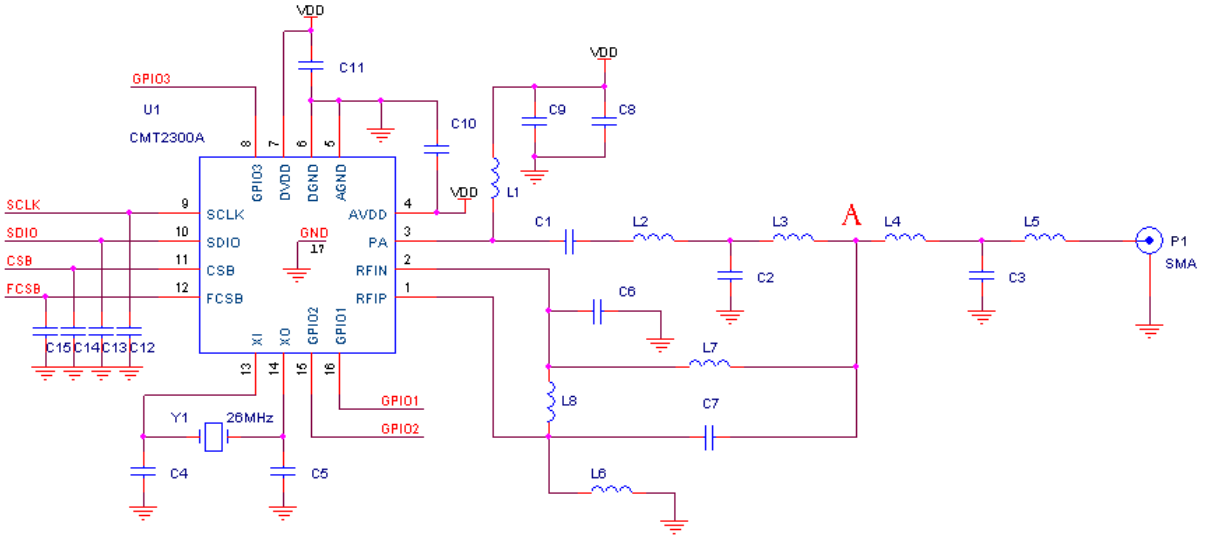


Figure 2. Direct tie application schematic diagram

Table 13. 13dBm direct tie application BOM

No.	Descriptions	Values			Unit	Supplier
		433 MHz +13 dBm	868 MHz +13dBm	915 MHz +13dBm		
C1	±5%, 0603 NP0, 50 V	15	22	22	pF	
C2	±5%, 0603 NP0, 50 V	5.6	6.2	6.2	pF	
C3	±5%, 0603 NP0, 50 V	7.5	3.6	3.3	pF	
C4	±5%, 0603 NP0, 50 V	24	24	24	pF	
C5	±5%, 0603 NP0, 50 V	24	24	24	pF	
C6	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C7	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C8	±5%, 0603 NP0, 50 V	4.7			uF	
C9	±5%, 0603 NP0, 50 V	470			pF	
C10	±5%, 0603 NP0, 50 V	0.1			uF	
C11	±5%, 0603 NP0, 50 V	0.1			uF	
L1	±5%, 0603 Multilayer chip inductor	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Multilayer chip inductor	56	10	8.2	nH	Sunlord SDCL
L3	±5%, 0603 Multilayer chip inductor	39	8.2	6.8	nH	Sunlord SDCL
L4	±5%, 0603 Multilayer chip inductor	18	10	8.2	nH	Sunlord SDCL
L5	±5%, 0603 Multilayer chip inductor	18	10	8.2	nH	Sunlord SDCL
L6	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L7	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L8	±5%, 0603 Multilayer chip inductor	68	12	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm		26		MHz	EPSON
U1	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver				-	CMOSTEK

Table 14. 20dBm direct tie application BOM

No.	Descriptions	Values			Unit	Supplier
		433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0603 NP0, 50 V	15	18	18	pF	
C2	±5%, 0603 NP0, 50 V	3.0	3.6	3.6	pF	
C3	±5%, 0603 NP0, 50 V	6.2	3.3	3.3	pF	
C4	±5%, 0603 NP0, 50 V	24	24	24	pF	
C5	±5%, 0603 NP0, 50 V	24	24	24	pF	
C6	±5%, 0603 NP0, 50 V	4.7	2	1.8	pF	
C7	±5%, 0603 NP0, 50 V	4.7	2	1.8	pF	
C8	±5%, 0603 NP0, 50 V	4.7			uF	
C9	±5%, 0603 NP0, 50 V	470			pF	
C10	±5%, 0603 NP0, 50 V	0.1			uF	
C11	±5%, 0603 NP0, 50 V	0.1			uF	
L1	±5%, 0603 Multilayer chip inductor	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Multilayer chip inductor,	22	12	12	nH	Sunlord SDCL
L3	±5%, 0603 Multilayer chip inductor	cap 15pF	15	15	nH	Sunlord SDCL
L4	±5%, 0603 Multilayer chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 Multilayer chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 Multilayer chip inductor	27	15	15	nH	Sunlord SDCL
L7	±5%, 0603 Multilayer chip inductor	27	15	15	nH	Sunlord SDCL
L8	±5%, 0603 Multilayer chip inductor	68	12	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	EPSON
U1	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver				-	CMOSTEK

3.2 RF Switch Type Schematic

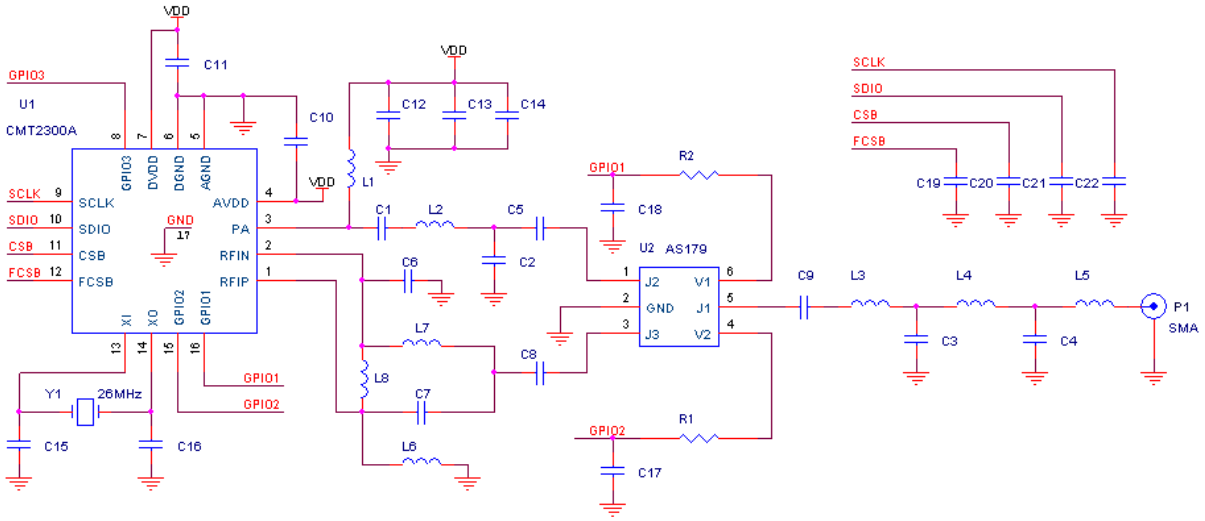


Figure 3. RF switch type application schematic diagram

Table 15. RF switch type application BOM

No.	Descriptions	Values		Unit	Supplier
		434 MHz +20 dBm	868 /915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	15	15	pF	
C2	±5%, 0402 NP0, 50 V	10	3.9	pF	
C3	±5%, 0402 NP0, 50 V	8.2	2.7	pF	
C4	±5%, 0402 NP0, 50 V	8.2	2.7	pF	
C5	±5%, 0402 NP0, 50 V	18 nH	220	pF	
C6	±5%, 0402 NP0, 50 V	4.7	2	pF	
C7	±5%, 0402 NP0, 50 V	4.7	2	pF	
C8	±5%, 0402 NP0, 50 V	220	220	uF	
C9	±5%, 0402 NP0, 50 V	220	220	pF	
C10	±5%, 0402 NP0, 50 V	0.1		uF	
C11	±5%, 0402 NP0, 50 V	0.1		uF	
C12	±5%, 0402 NP0, 50 V	470		pF	
C13	±5%, 0402 NP0, 50 V	2200		pF	
C14	±5%, 0402 NP0, 50 V	4.7		uF	
C15	±5%, 0402 NP0, 50 V	24	24	pF	
C16	±5%, 0402 NP0, 50 V	24	24	pF	
C17	±5%, 0402 NP0, 50 V	10	10	pF	
C18	±5%, 0402 NP0, 50 V	10	10	pF	
C19	±5%, 0402 NP0, 50 V	27		pF	
C20	±5%, 0402 NP0, 50 V	27		pF	
C21	±5%, 0402 NP0, 50 V	27		pF	
C22	±5%, 0402 NP0, 50 V	27		pF	
L1	±5%, 0603 Multilayer chip inductor	180	100	nH	Sunlord SDCL
L2	±5%, 0402 Multilayer chip inductor	27	6.8	nH	Sunlord SDCL
L3	±5%, 0402 Multilayer chip inductor	18	12	nH	Sunlord SDCL

No.	Descriptions	Values		Unit	Supplier
		434 MHz +20 dBm	868 /915 MHz +20 dBm		
L4	±5%, 0402 Multilayer chip inductor	33	22	nH	Sunlord SDCL
L5	±5%, 0402 Multilayer chip inductor	15	10	nH	Sunlord SDCL
L6	±5%, 0402 Multilayer chip inductor	27	12	nH	Sunlord SDCL
L7	±5%, 0402 Multilayer chip inductor	27	12	nH	Sunlord SDCL
L8	±5%, 0402 Multilayer chip inductor	68	18	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26		MHz	EPSON
U1	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver	-		-	CMOSTEK
U2	AS179, PHEMT GaAs IC SPDT Switch	-		-	SKYWORKS
R1	±5%, 0402	2.2		kΩ	
R2	±5%, 0402	2.2		kΩ	

4. Function Descriptions

CMT2300A is an ultra low power, high performance transceiver chip. It supports OOK, (G) FSK, (G) MSK RF suitable for applications ranging from 140 to 1020MHz. The product belongs to CMOSTEK NextGenRFTM series. The series includes transmitters, receivers and transceivers and other complete product lines. CMT2300A block diagram is as shown in the following figure.

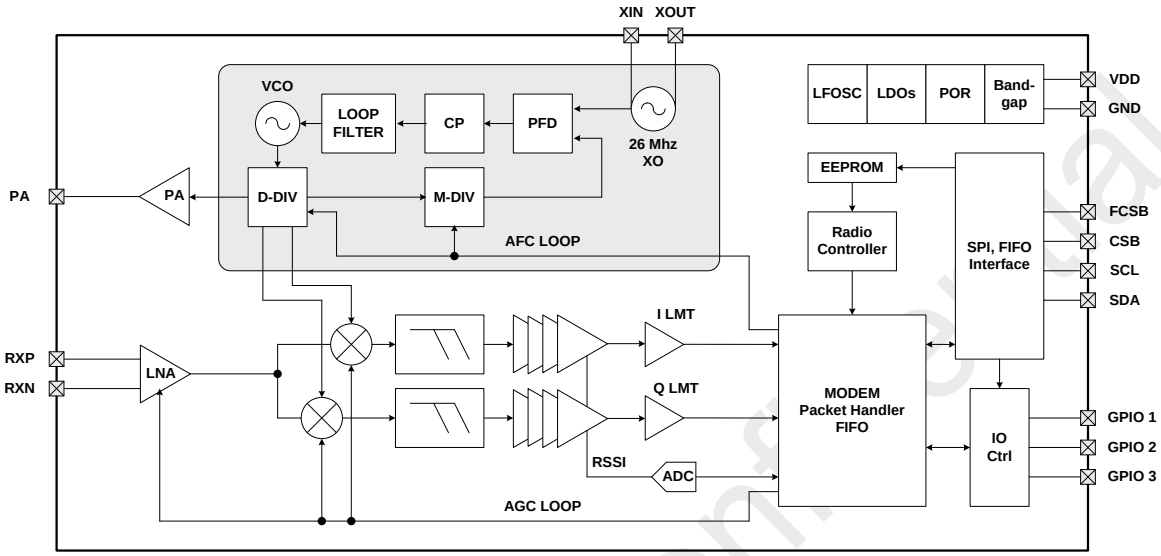


Figure 4. Functional Block Diagram

In the receiver part, the chip uses the LNA+MIXER+IFFILTER+LIMITTER+PLL low-IF structure to achieve the wireless reception function with the frequency below 1G, and uses the PLL+PA structure to achieve the wireless transmission function with the frequency below 1G.

In the receiver system, the analog circuit is responsible for mixing the RF signal to the intermediate frequency, and transferring IF signal from analog to digital by Limiter module, and outputting I/Q two single bit signal to a digital circuit to do follow-up (G) FSK demodulation. At the same time, the circuit will convert the real-time RSSI signal into 8-bit digital signal by ADC, and send them to the digital part for OOK demodulation and other processing. Digital circuit is responsible for mixing the intermediate frequency signal to zero frequency (Baseband) and carrying out a series of filtering and decision processing, and dynamically controlling analog circuits by AFC and AGC, finally demodulating the original 1-bit signal. After demodulation, the signal will be sent to the decoder to decode and fill in the FIFO, or directly output to PAD.

In the transmitter system, the digital circuit encodes the data and processes it, and sends them to the modulator (and also sends them directly to the modulator). The modulator will directly control the PLL and PA, modulate the data with (G) FSK or OOK and transmit them.

4.1 Transmitter

CMT2300A is based on RF frequency directly integrated transmitter. The carrier is generated by a low noise fractional-N frequency synthesizer.

The modulated data is transmitted by an efficient single ended power amplifier (PA). The output power can be read and written by register, step by step from -20dBm to +20dBm with 1dB.

When the PA is switched fast, the varying input impedance will disturb the output frequency of the VCO instantaneously. The

effect is called VCO pulling. It will generate the spurious and spurs on the spectrum around the desired carrier. The PA spurs can be reduced to a minimum instantaneously by the PA output power ramping. CMT2300A has built-in PA ramping mechanism. When the PA Ramp is turned on, the PA output power can ramp the desired amplitude by setting the rate, so as to reduce the spectral components.

According to different application requirements, the user can design a PA matching network to optimize the transmitting efficiency under the required output power. The typical application schematic and the required BOM see Chapter third "Typical application schematic". For more schematic details and layout guidelines, please refer to“ AN141 CMT230xA Schematic and PCB Layout Design Guideline”.

The transmitter can operate in direct mode and package mode. In the direct mode, the data to be transmitted can be input the chip by the DIN pin and transmitted directly. In the package mode, the data can be pre-loaded into the chip FIFO in STBY, TFS and Tx States, and be transmitted together with other package elements.

4.2 Receiver

CMT2300A has a built-in ultra low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog module is calibrated to the internal reference voltage. This allows the chip to work better at different temperatures and voltages. Baseband filtering and demodulation can be completed by the digital demodulator. When the chip is working in the environment of large interference signal below the bandwidth, the AGC loop adjust the system gain by the broadband power detector and attenuation network nearby LNA, so as to obtain the best system linearity, selectivity, sensitivity and other performance.

Leveraging CMOSTEK's low power design technology, the receiver consumes only a very low power when it is open. The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application of strict requirements for power consumption.

Similar to the transmitter, the CMT2300A receiver can operate in direct mode and packet mode. In the direct mode, the demodulator output data can be directly output through the DOUT pin of the chip. DOUT can be configured by GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet processor and decoded, and then is filled in the FIFO. MCU can read FIFO by the SPI interface.

4.3 Auxiliary Blocks

4.3.1 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop and provides a system clock for the digital module. The load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL, so as to make the crystal accurately oscillate at 26 MHz.

$$C_L = \frac{1}{1/C15 + 1/C16} + C_{par} + 2.5pF$$

C15 and C16 are load capacitances at both ends of the crystal. Cpar is parasitic capacitance on PCB. For the chip internal 5pF capacitance, the difference is equivalent to 2.5pF. The equivalent series resistance of the crystal should be within the specified specifications so that the crystal can have a reliable vibration. An external signal source can also be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300mV to 700mV. A capacitor is couple to X1 pin.

4.3.2 Sleep Timer

The CMT2300A integrates a sleep timer driven by 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer wakes the chip from sleep periodically. When the chip operates in a cycle mode, the sleep time can be configured from 0.03125 ms to 41922560 ms. Due to the low power oscillator frequency will change with the temperature and voltage drift, it will be automatically calibrated during power on and will be periodically calibrated. These calibrations will keep the frequency tolerance of the oscillator within + 1%.

4.3.3 Low Battery Detection

The chip sets up low voltage detection. When the chip is tuned to a certain frequency, the test is performed once. Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state, Test results can be read by the LBD_VALUE register.

If the LBD_STOP_EN is set to 1, the chip will stop at the LOW_VDD (CHIP_MODE_STA<3:0> = 1000, Addr=0x61) stage when the supply voltage is below the predetermined value. The chip is waiting for the order that MCU allow the chip to switch to SLEEP or Standby mode by SPI.

4.3.4 Received Signal Strength Indicator (RSSI)

RSSI is used to evaluate the signal strength within the tuned channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The logarithmic amplifier of I channels and Q channel contains the received signal indicator. The DC voltage is proportional to the input signal strength. The output of RSSI is the sum of two signal values. Dynamic range extends from the sensitivity level to 80dB above. After the signal intensity is sampled by ADC, the smoother RSSI value is obtained by smoothing filtering. The filter order can be set by RSSI_AVG_MODE<2:0> (Addr=0x16). The code value is translated into dBm value after filtering. Users can read the register to obtain the corresponding RSSI code value（RSSI_CODE<7:0>, Addr=0x6F）or dBm value（RSSI_DBM<7:0>, Addr=0x70）.

CMT2300A has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, the user needs to recalibrate in actual use. For the specific use method, please refer to the relevant AN documents.

4.3.5 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in FSK demodulation, the user can observe the jump characteristics of the received signal to determine whether the incoming noise or useful signal. PJD believes that the input signal from 0 to 1 or from 1 to 0 switching is a phase jump. Users just need to configure the PJD_WIN_SEL<1:0> (Addr=0x17) to tell PJD how many times the signal changes to determine the results of the output.

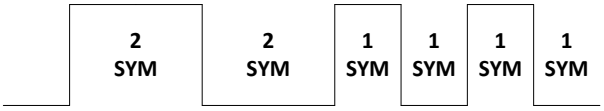


Figure 5. Received signal jump diagram

As shown above, total 8 symbols are received. But the jump only appeared 6 times. Therefore, the jump variables are not equal to the number of symbol. Only when the preamble is received, the jump variables are equal to the number of symbol. Users need to pay attention to this point.

PJD can be used to achieve ultra low power (SLP) receive mode. In general, the more the number of PJD jumps, the more reliable the judgment results are; the less, the faster it is done. If the time interval is very short, it is necessary to reduce the number of detection to meet the setting requirements. In general, 4 jumps have been able to achieve the more reliable test

results. Do not mistake the noise as a useful signal. Detect the useful signal when the signal is coming.

4.3.6 Fast Frequency Hopping

In the application of multi channels, users don't need to configure the complex register for changing the frequency every time, only need to configure a register on the base frequency.

$$\mathbf{FREQ} = \mathbf{BASE\ FREQUENCY} + \mathbf{2.5\ kHz} \times \mathbf{FH\_OFFSET} < \mathbf{7:0} > \times \boldsymbol{FH\_CHANNEL} < \mathbf{7:0} >$$

In general, the user can configure FH_OFFSET<7:0> (Addr=0x64) during the power on initialization. And then in the application, the user can switch the channel by changing FH_CHANNEL<7:0> (Addr=0x63) frequently.

5. Chip Operation

5.1 SPI Interface

MCU communicates with the chip by 4 wire SPI interface. MCU can access the chip register when CSB is low level. MCU can access the chip FIFO when FCSB is low level. CSB and FCSB cannot be low level simultaneously. SCLK is the serial clock. For the MCU and the chip, data is always transmitted on the falling edge of the SCLK, and is sampled on the rising edge. SDIO is a bidirectional data pin. Addresses and data are always sent from MSB.

When MCU accesses the register, it sends a R/W (read / write) bit, followed by a 7 bit register address. Before sending the R/W bit, the MCU must pull the CSB low for at least half a SCLK cycle. After sending the last SCLK falling edge, the MCU must wait at least half of the SCLK cycle and then pull the CSB again.

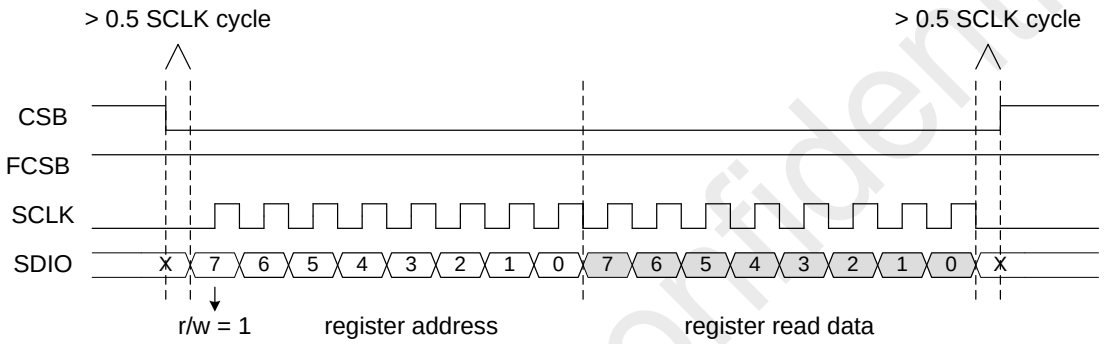


Figure 6. SPI read register timing

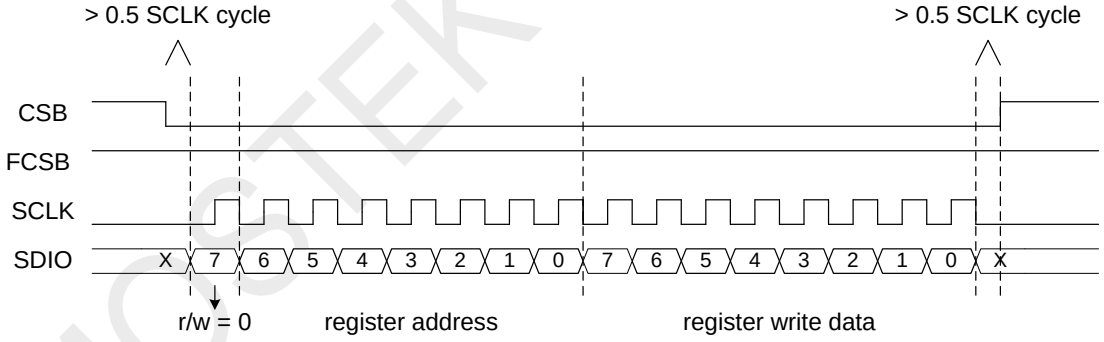


Figure 7. SPI write register timing

5.2 FIFO

FIFO is used to store the received data in Rx mode, and to store the transmitting data in Tx mode. FIFO can be read by the SPI interface. The user can clear FIFO by setting FIFO_CLR_TX/RX (Addr=0x6C).. Also, the user can repeatedly send the filled data previously by setting FIFO_RESTORE. No need to fill in the data again.

By setting the register FIFO_MERGE_EN (Addr=0x69), the user can choose to use a 32 bytes FIFO specifically for the Rx mode and another 32 bytes FIFO for Tx mode, or by merging two 32 bytes FIFOs into one 64 bytes FIFO for Tx or Rx mode. When the FIFO is 64 bytes, it indicates that the maximum number of bytes that can be stored in the chip is 64 bytes. If you do not merge them, while you fill in the 32 bytes Rx FIFO, you can also fill in the 32 bytes Tx FIFO for the next sending at the same, so as to save the system operating time.

5.2.1 FIFO Read Operation

When reading data from the FIFO, each read a byte, the internal read pointer will automatically add 1.MCU must pull FCSB down for a SCLK cycle to release the rising edge of the first SCLK. After sending the last SCLK falling edge, the MCU must wait for at least 2us to pull the FCSB back to the high level. Also, before reading the next byte of the FIFO, the FCSB needs to be pulled up for at least 4us. It allows the chip to generate the corresponding FIFO interrupt according to the status.

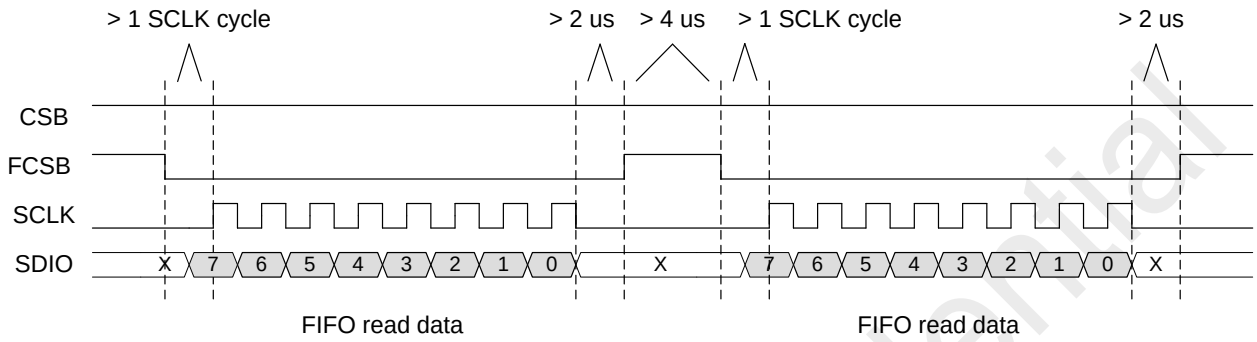


Figure 8. SPI read FIFO timing

5.2.2 FIFO Write Operation

When writing to FIFO, each write a byte, the internal read pointer will automatically add 1.SDIO data is collected on the rising edge of SCLK. MCU must pull FCSB down for a SCLK cycle to release the rising edge of the first SCLK. After sending the last SCLK falling edge, the MCU must wait for at least 2us to pull the FCSB back to the high level. Also, before writing the next byte of the FIFO, the FCSB needs to be pulled up for at least 4us. It allows the chip to generate the corresponding FIFO interrupt according to the status.

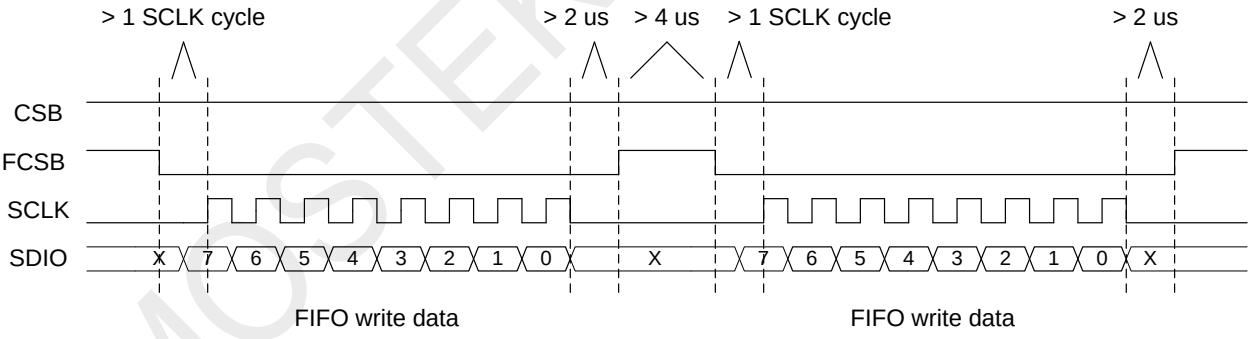


Figure 9. SPI write FIFO timing

5.2.3 FIFO Associated Interrupt

CMT2300A provides rich interrupt sources associated with the FIFO. As an auxiliary means of the efficient operation, FIFO interrupt timing associated with Tx and Rx is as shown below.

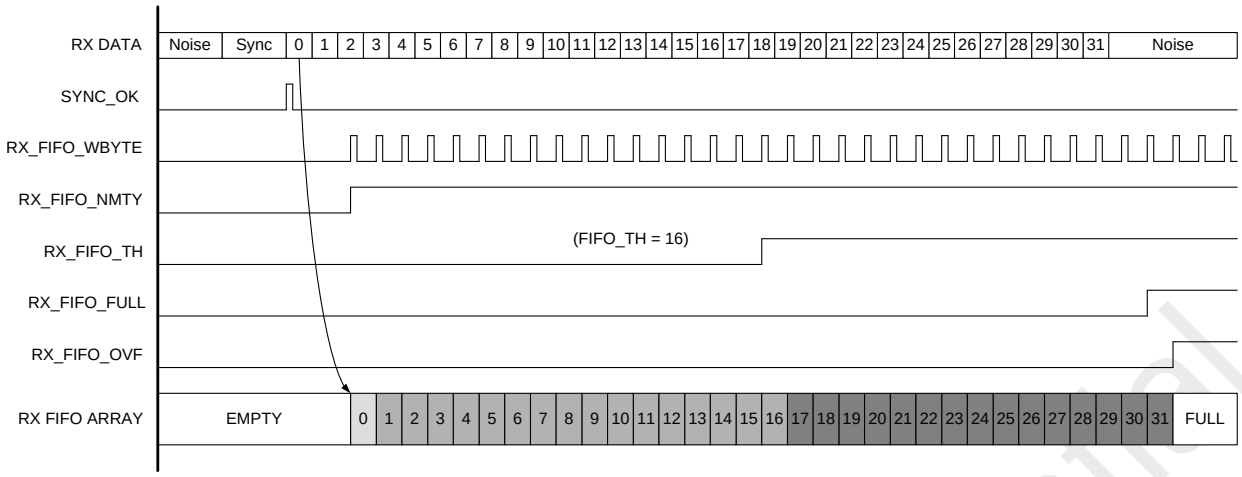


Figure 10. CMT2300ARX FIFO interrupt timing diagram

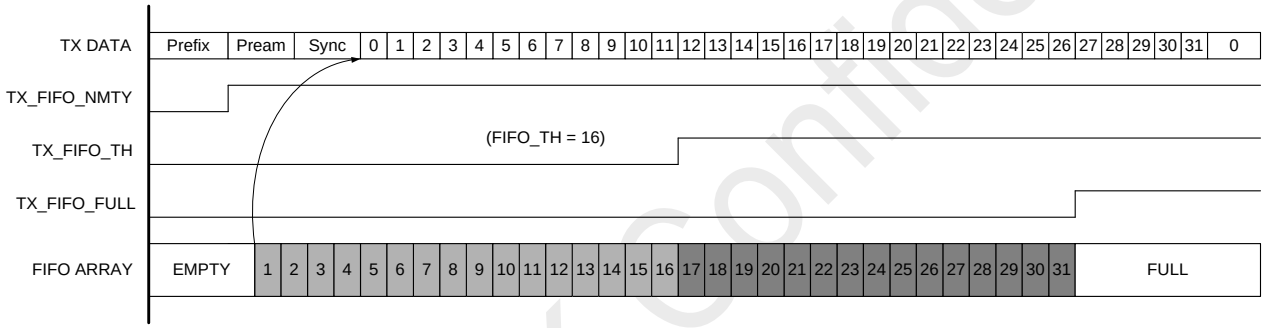


Figure 11. CMT2300A TX FIFO interrupt timing diagram

5.3 Operation State, Timing and Power Consumption

5.3.1 Startup Timing

The chip usually needs to wait about 1ms after VDD is powered on, and then to release POR. After the release of POR, the crystal will start .up. The startup time default is Nms according to the crystal itself. After starting, you need to wait for crystal stabilization, and then the system will start running. The default stabilization time is 2.48ms. The time can be modified by writing XTAL_STB_TIME <2:0> (Addr=0x0E). The chip remains in the IDLE state until the crystal is stable. After the crystal stability, the chip will leave the IDLE and began to do the calibration of each module. After the calibration is completed, the chip will stay in the SLEEP and wait for the user to initialize the configuration. At any time, as long as the chip is reset, it will go back to the IDLE and be powered on again.

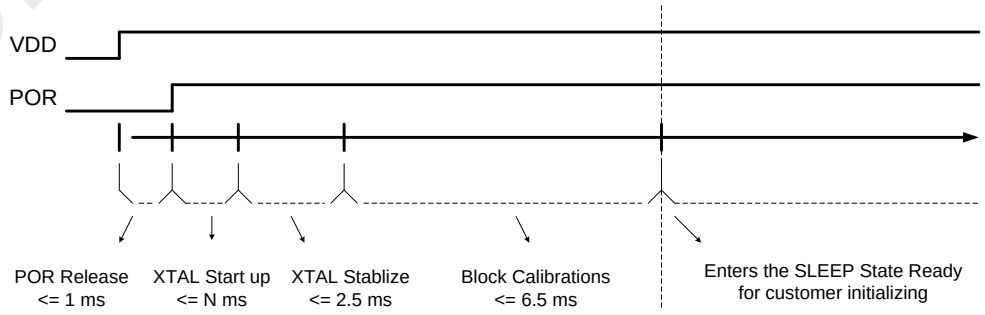


Figure 12. Power on sequence

When the calibration is completed, the chip enters the SLEEP mode. From this time, the MCU can switch the chip to different operating state by setting the register CHIP_MODE_SWT<7:0>（Addr=0x60）.

5.3.2 Operation State

CMT2300A has 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown below.

Table 16. CMT2300A state and module open table

State	Binary code	Switch command	Open module	Open methods
IDLE	0000	soft_rst	SPI, POR	None
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
RFS	0011	go_rfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
RX	0101	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+IF, FIFO	CLKO, RX Timer
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

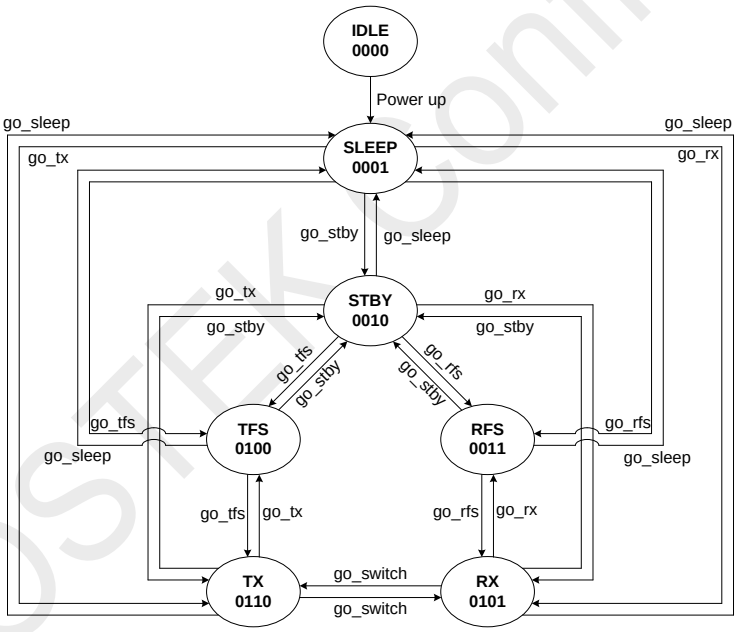


Figure 13. State Switch Diagram

■ SLEEP State

The power consumption of the chip is the lowest in SLEEP mode. Almost all modules are closed. SPI is open. The register of the configuration area and control area 1 can be accessed. The contents filled in FIFO before will be remained. But FIFO cannot be operated. If the user opens a timed wake-up function, the LFOSC and the sleep timer will turn on and work. The required time to switch from IDLE to SLEEP is the power on time as shown above. Switching from the other state to SLEEP will be completed immediately.

■ STBY State

In the STBY state, the crystal is turned on, the LDO of the digital circuit will also be turned on, the current will be slightly increased. FIFO can be operated. The user can choose whether to output the CLKO (system clock) to the GPIOn pin. Because

the crystal has been turned on, the time from STBY to transmitting or received state is less than from SLEEP state to transmitting or received state. Switching from SLEEP to STBY needs to wait until the crystal is turned on and stable. Switching from other state to STBY will be completed immediately.

■ RFS State

RFS is a transition state before switching to RX. In addition to the receiver RF module is closed, the other modules are open. The current will be larger than in STBY. RFS cannot be switched to Tx because the PLL has been locked in the Rx frequency. Switching from STBY to RFS needs about 350us to calibrate and stabilize PLL. Switching from SLEEP to RFS needs to add the time that crystal is started and stabilized. Switching from other state to RFS will be completed immediately.

■ TFS State

TFS is a transition state before switching to TX. In addition to the transmitter RF module is off, the other modules are open. The current will be larger than in STBY. TFS cannot be switched to Rx state because the PLL has been locked in the Tx frequency. Switching from STBY to TFS needs about 350us to calibrate and stabilize PLL. Switching from SLEEP to TFS needs to add the time that crystal is started and stabilized. Switching from other state to TFS will be completed immediately.

■ RX State

All modules about the receiver will be opened in RX. Switching from RFS to RX requires only 20us.Switching from STBY to RX needs to add 350us to calibrate and stabilize PLL. Switching from SLEEP to RX needs to add the time that crystal is started and stabilized. TX can be quickly switched to RX by sending “go_switch” command. Whether TX or RX is set the same frequency, switching successfully needs 350us that the PLL is calibrated and stabilized again.

■ TX State

All modules about the transmitter will be opened in TX. Switching from TFS to TX requires only 20us.Switching from STBY to TX needs to add 350us to calibrate and stabilize PLL. Switching from SLEEP to RX needs to add the time that crystal is started and stabilized. RX can be quickly switched to TX by sending “go_switch” command. Whether RX or TX is set the same frequency, switching successfully needs 350us that the PLL is calibrated and stabilized again. It should be noted that switching directly between RX and TX state only use the “go_switch” command.

5.4 GPIO and Interrupt

CMT2300A has 3 GPIO ports. Each GPIO can be configured as a different input or output. CMT2300A has 2 interrupt ports. They can be configured to different GPIO outputs.

Table 17. CMT2300A GPIO

Pin No.	Name	I/O	Function
16	GPIO1	IO	Configured as:DOUT/DIN, INT1, INT2, DCLK (TX/RX), RF_SWT
15	GPIO2	IO	Configured as:INT1, INT2, DOUT/DIN, DCLK (TX/RX), RF_SWT
8	GPIO3	IO	Configured as:CLKO, DOUT/DIN, INT2, DCLK (TX/RX)

Interrupt mapping table is as below. INT1 and INT2 mapping is the same. Take INT1 as an example.

Table 18. CMT2300A interrupt mapping table

Name	INT1_SEL	Descriptions	Clearing methods
RX_ACTIVE	00000	Ready to enter RX. It is 1 in PLL and RX state, and it is 0 in the other state.	Auto
TX_ACTIVE	00001	Ready to enter TX. It is 1 in PLL and TX state, and it is 0 in the other state.	Auto
RSSI_VLD	00010	Indicates whether the RSSI is active.	Auto
PREAM_OK	00011	Indicates that the Preamble interrupt is received successfully.	by MCU
SYNC_OK	00100	Indicates that the Sync Word interrupt is received successfully.	by MCU
NODE_OK	00101	Indicates that the Node ID interrupt is received successfully.	by MCU
CRC_OK	00110	Indicates that the interrupt is successfully received and verified by CRC.	by MCU
PKT_OK	00111	Indicates that a packet interrupt has been received.	by MCU
SL_TMO	01000	Indicates that the SLEEP counter timed out.	by MCU
RX_TMO	01001	Indicates that the RX counter timed out.	by MCU
TX_DONE	01010	Indicates that the TX is completed.	by MCU
RX_FIFO_NMTY	01011	Indicates that the RX FIFO is not empty.	Auto
RX_FIFO_TH	01100	Indicates unread RX FIFO is over FIFO TH	Auto
RX_FIFO_FULL	01101	Indicates RX FIFO is filled.	Auto
RX_FIFO_WBYTE	01110	Indicates the byte written to RX FIFO is a pulse.	Auto
RX_FIFO_OVF	01111	indicates RX FIFO is overflow	Auto
TX_FIFO_NMTY	10000	Indicates that TX FIFO is not empty	Auto
TX_FIFO_TH	10001	Indicates unread TX FIFO is over FIFO TH.	Auto
TX_FIFO_FULL	10010	Indicates TX FIFO is full.	Auto
STATE_IS_STBY	10011	Indicates that the current state is STBY.	Auto
STATE_IS_FS	10100	Indicates that the current state is RFS or TFS.	Auto
STATE_IS_RX	10101	Indicates that the current state is RX.	Auto
STATE_IS_TX	10110	Indicates that the current state is TX.	Auto
LBD	10111	Indicates that low battery detection is effective（VDD is lower than TH）	Auto
TRX_ACTIVE	11000	Ready to enter TX or RX. It is 1 in PLL, TX or RX state, and it is 0 in the other state.	Auto
PKT_DONE	11001	Indicates that the current packet has been received, as shown below. 1. Receives the packet completely. 2. Chester decoding is error. Decoding circuit automatically restarts. 3. NODE ID receiving is error. Decoding circuit automatically restarts. 4. Signal is conflict. Decoding circuit does not restart automatically, waiting for MCU processing.	by MCU

Interrupt default is 1 valid. But you can set the INT_POLAR (Addr=0x66) register bit to 1 to make all interrupts valid for 0.Taking INT1 as an example, the control and selection diagram for all interrupt sources is drawn. For the control and mapping, INT1 and INT2 are the same.

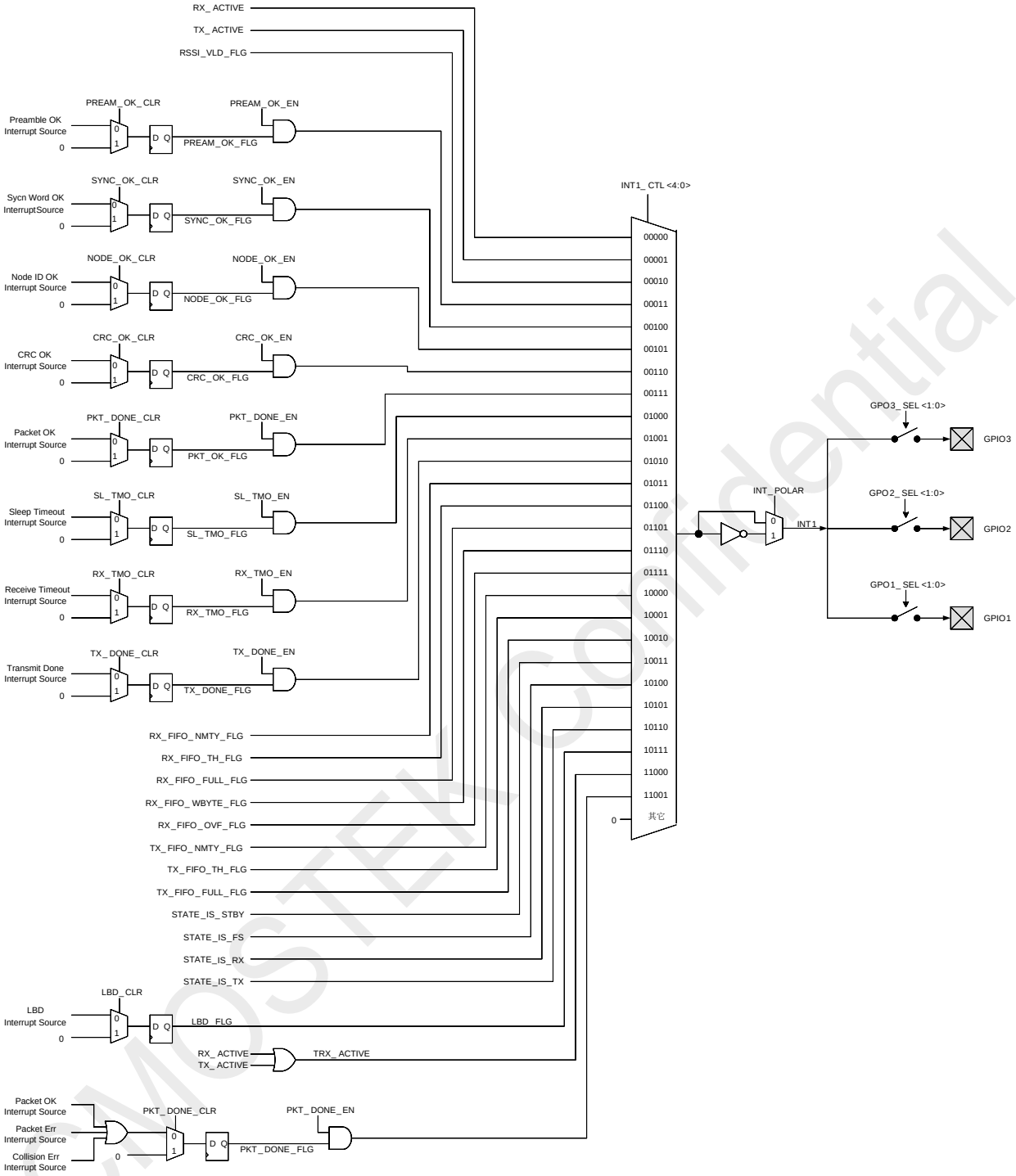


Figure 14. CMT2300A INT1 interrupt mapping diagram

6. Data Packet and Packet Handler

6.1 Packet Format

CMT2300A uses TX and RX unified configuration, more typical, more flexible packet format. It includes variable packet (Length in front of the Node ID), variable packet (Length in the back of the Node ID) and fixed packet, as shown below.

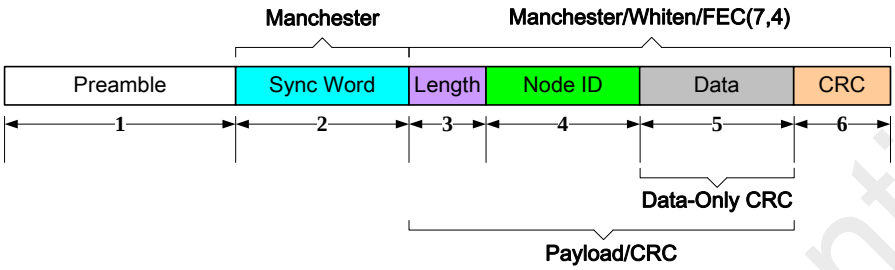


Figure 15. Variable length packet (Length in front of Node ID)

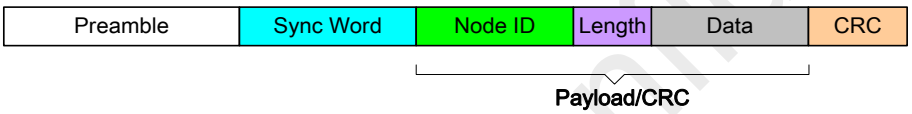


Figure 16. Variable length packet (Length behind Node ID)

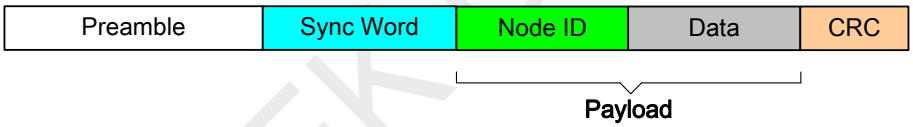


Figure 17. Fixed length packet

6.2 Data Mode

Data Mode refers to the external MCU transmits or receives the data in some way. CMT2300A supports direct mode and packet mode, the difference is as below.

- Direct – Direct mode --Only supports preamble and sync detection, FIFO does not work
- Packet – Packet mode --Supports all packet formats, FIFO works

6.2.1 Direct Mode

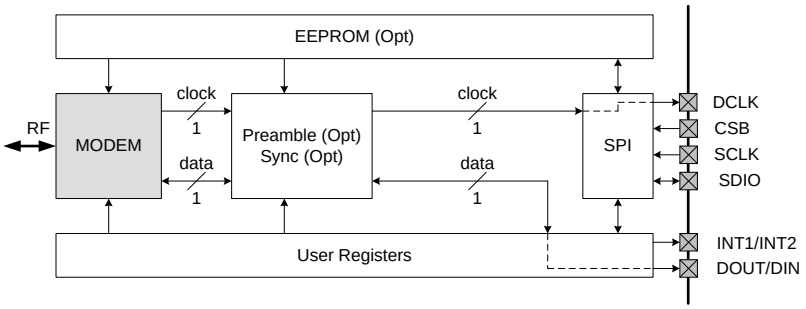


Figure 18. Direct mode data path

Rx processing

In the direct mode, the data from the demodulator is sent directly to the external MCU by the DOUT pin. DOUT can be set to GPIO1, 2 or 3.The typical direct mode Rx working timing is as below.

1. Configures GPIOs by CUS_IO_SEL (Addr=0x65) register.
2. Configures DATA_MODE = 0（Addr=0x38）.
3. Sends go_rx command.
4. Receives the dada from DOUT continuously.
5. Sends go_sleep/go_stby/go_rfs command to save power.

Tx processing

In the direct mode, the data to be transmitted is sent directly to the chip from the external MCU by the DIN pin. The data rate can be set by the MCU as long as it is in the chip specification. And if the chip uses GFSK modulation, you need to configure the data rate in advance, and the data rate to be transmitted by MCU is within the specified tolerance range. The typical direct mode Tx working timing is as below.

1. Register TX_DIN_EN (Addr=0x69) is set to 1 to enable GPIO DIN
2. TX_DIN_SEL（Addr=0x69）is set to 0 to configure GPIO1 as DIN, or is set to 1 to configure GPIO2 as DIN.
3. Drives DIN pin with logic 0 or 1.
4. Sends go_tx command, the chip starts sending the data from DIN pin.
5. Sends data to DIN pin continuously, the data is immediately sent out.
6. Sends go_sleep/go_stby/go_rfs command to save power.

6.2.2 Packet Mode

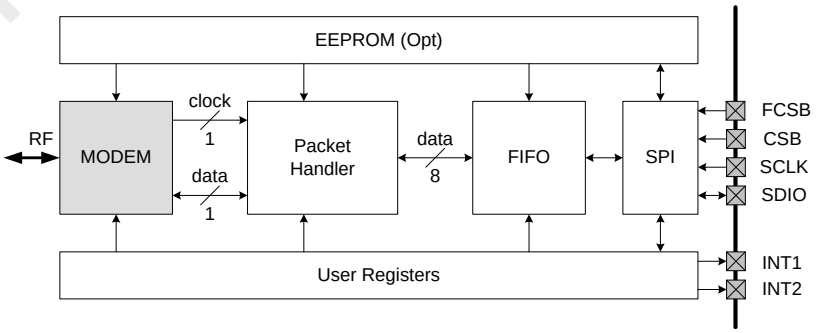


Figure 19. Packet mode data path

Rx processing

In the packet mode, the output data from the demodulator will be transferred to the packet handler for decoding, and then be filled in the FIFO. The packet handler provides a variety of decoding engines and options to determine the validity of the data. These can reduce the user's MCU resources. The typical package mode Rx working timing is as below.

1. Configures GPIO by CUS_IO_SEL (Addr=0x65).
2. Sets interrupt by CUS_INT1_CTL(Addr=0x66), CUS_INT2_CTL(Addr=0x67)和CUS_INT_EN(Addr=0x68).
3. Sends go_rx command
4. Reads FIFO according to the relevant interrupt status.
5. Sends go_sleep/go_stby/go_rfs command to save power.
6. Clears the packet interrupt status by CUS_ INT_CLR1/2(Addr=0x6A/B).

Tx processing

In the packet mode, MCU can fill the data in the FIFO in advance in the STBY and TFS state, or fill them in the FIFO while the chip sends the data, or use the combination of the above two methods. The typical packet mode Tx working timing is as below.

1. Configures GPIO by CUS_IO_SEL (Addr=0x65)
2. Sends go_stby/go_tfs command when the data is filled in FIFO in advance.
3. Sends go_tx command.
4. Writes the data into FIFO according to the relevant interrupt status.
5. Sends go_sleep/go_stby/go_rfs command to save power.

7. Low Power Operation

7.1 Duty Cycle Operation Mode

CMT2300A makes the Tx and Rx work in duty cycle operation mode to save chip power consumption by configuring the relevant registers. Among them, the Rx Duty Cycle can be divided into the following 5 modes.

1. Full manual control
2. Auto SLEEP awake
3. Automatic SLEEP wake up, automatic access to RX.
4. Automatic SLEEP wake up, automatic exit RX.
5. Automatic reception

The Tx Duty Cycle can be divided into the following 3 modes.

1. Automatic exit TX
2. Automatic SLEEP wake up, automatic exit TX
3. Automatic transmission

7.2 Supper Low Power (SLP) Receive Mode

CMT2300A provides a series of options to help users achieve supper low power consumption (SLP - Supper Low Power) reception under different application requirements. These options must be set to 1 in RX_TIMER_EN that they will take effect when the Rx timer is valid. The core content of the SLP receiver is how to shorten the Rx time when there is no signal and properly extend the Rx time when there is signal. Finally, the power consumption is minimized and the effect is stable.

The traditional short-range wireless transceiver system generally uses the following basic scheme to achieve low power transceiver.CMT2300A is also compatible with this scheme, and extends 13 more power saving schemes on the basis. Here to introduce the most basic scheme. That is, the scheme will be achieved when the RX_EXTEND_MODE<3:0> is set to 0.

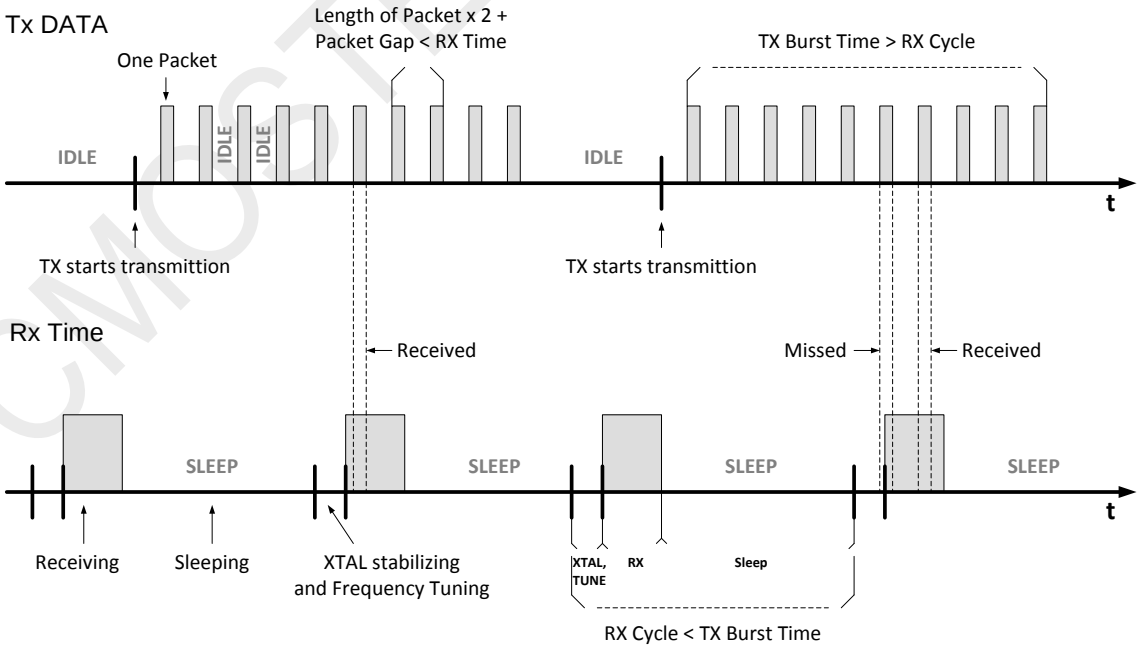


Figure 20. Basic low-power transceiver scheme

The traditional low-power transceiver scheme and the 13 extended low-power schemes based on it are listed in the following table.

Table 19. Low-power transceiver mode

No.	Rx Extended Methods	Rx Extended Condition
0	Don't delay if 0 is configured. Leave Rx as long as T1 timed out.	None
1	Once meet the condition during T1, leave T1 and give the control power to MCU.	RSSI_VLD is valid.
2		PREAM_OK is valid.
3		RSSI_VLD and PREAM_OK are valid simultaneously.
4	Once detect RSSI valid during T1, leave T1 and in Rx state, and exit Rx until RSSI is not satisfied.	RSSI_VLD is valid.
5	Once meet the condition during T1, switch to T2. Leave Rx as long as T2 timed out.	RSSI_VLD is valid
6		PREAM_OK is valid
7		RSSI_VLD and PREAM_OK are valid simultaneously.
8		Any one of PREAM_OK or SYNC_OK is valid.
9		Any one of PREAM_OK or NODE_OK is valid.
10		Any one of PREAM_OK or SYNC_OK or NODE_OK is valid.
11	Once meet the condition during T1, switch to T2. Leave T2 and give the control power to MCU as long as SYNC is detected, otherwise exit Rx when T2 timed out.	RSSI_VLD is valid.
12		PREAM_OK is valid.
13		RSSI_VLD 与 PREAM_OK are valid simultaneously.

The T1 and T2 mentioned in the table refer to the RX T1 and the T2 time interval that can be set in the register. For the specific low power setting, please refer to the relevant technical documents.

8. User Register

The register list is given below. For the register specific use, please refer to the AN146 CMT2300A manual. These register partitions, in addition to the control bank2 cannot be accessed under the SLEEP state, the others can be accessed under the SLEEP state.

Table 20. Register Banks

Address range	Name		RFPDK	Remark
0x00~0x0B	Configuration bank(the configuration values can be exported by the Export function of the RFPDK software)	Internal parameter bank	CMT Bank	Exported by RFPDK, does not recommend to be modified by customers.
0x0C~0x17		System operation bank	System Bank	The bank mainly involves the Duty Cycle configuration.
0x18~0x1F		Frequency configuration bank	Frequency Bank	The bank configures transmit and receive frequency.
0x20~0x37		Data rate bank	Data Rate Bank	The bank involves the communication rate and configures the receive parameters for the rate and deviation.(demodulation / bandwidth)
0x38~0x54		Baseband bank	Baseband Bank	The bank involves the packet structure.(Coding format, message structure, verification, error correction, synchronization, etc.)
0x55~0x5F		Tx parameter bank	TX Bank	The bank involves the transmit frequency offset and power.
0x60~0x6A	Control bank 1 (Configured according to MCU requirements, not generated by RFPDK)		--	Operation state, frequency hopping configuration, GPIO configuration, interrupt source switch, etc.
0x6B~0x71	Control bank 2 (Configured according to MCU requirements, not generated by RFPDK)		--	Interrupt source flag, FIFO control, RSSI measurement, etc.

8.1 CMT Bank

The CMT bank mainly stores the information about the product and other functional registers, and also contains a number of registers used inside the chip.

Table 21. CMT Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	RW	CUS_CMT1	User does not need to understand the detail, just directly export the register contents from the RFPDK							
0x01	RW	CUS_CMT2								
0x02	RW	CUS_CMT3								
0x03	RW	CUS_CMT4								
0x04	RW	CUS_CMT5								
0x05	RW	CUS_CMT6								
0x06	RW	CUS_CMT7								
0x07	RW	CUS_CMT8								
0x08	RW	CUS_CMT9								
0x09	RW	CUS_CMT10								
0x0A	RW	CUS_CMT11								
0x0B	RW	CUS_RSSI								

8.2 System Bank

The system bank mainly configures the parameters about the timer to achieve Duty Cycle and ultra low power mode.

Table 22. System Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	RW	CUS_SYS1	LMT_VTR [1:0]		MIXER_BIAS [1:0]		LNA_MODE [1:0]		LNA_BIAS [1:0]	
0x0D	RW	CUS_SYS2	LFOSC_RECAL_EN	LFOSC_CAL1_EN	LFOSC_CAL2_EN	RX_TIMER_EN	SLEEP_TIMER_EN	TX_DC_EN	RX_DC_EN	DC_PAUSE
0x0E	RW	CUS_SYS3	SLEEP_BYPASS_EN	XTAL_STB_TIME [2:0]			TX_EXIT_STATE [1:0]		RX_EXIT_STATE [1:0]	
0x0F	RW	CUS_SYS4	SLEEP_TIMER_M [7:0]							
0x10	RW	CUS_SYS5		SLEEP_TIMER_M [10:8]			SLEEP_TIMER_R [3:0]			
0x11	RW	CUS_SYS6	RX_TIMER_T1_M [7:0]							
0x12	RW	CUS_SYS7		RX_TIMER_T1_M [10:8]			RX_TIMER_T1_R [3:0]			
0x13	RW	CUS_SYS8	RX_TIMER_T2_M [7:0]							
0x14	RW	CUS_SYS9		RX_TIMER_T2_M [10:8]			RX_TIMER_T2_R [3:0]			
0x15	RW	CUS_SYS10	COL_DET_EN	COL_OFS_SEL	RX_AUTO_EXIT_DIS	DOUT_MUTE	RX_EXTEND_MODE [3:0]			
0x16	RW	CUS_SYS11	PJD_TH_SEL	RSSI_VLD_SRC [1:0]		RSSI_DET_SEL [1:0]		RSSI_AVG_MODE [2:0]		
0x17	RW	CUS_SYS12	PJD_WIN_SEL [1:0]		RESV	RESV				

8.3 Frequency Bank

The frequency bank mainly stores the register with frequency tuning function.

Table 23. Frequency Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18	RW	CUS_RF1	User does not need to understand the detail, just directly export the register contents from the RFPDK							
0x19	RW	CUS_RF2								
0x1A	RW	CUS_RF3								
0x1B	RW	CUS_RF4								
0x1C	RW	CUS_RF5								
0x1D	RW	CUS_RF6								
0x1E	RW	CUS_RF7								
0x1F	RW	CUS_RF8								

8.4 Data Rate Bank

Data rate bank mainly stores data rate related, FSK related and OOK related registers.

Table 24. Data Rate Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	RW	CUS_RF9	User does not need to understand the detail, just directly export the register contents from the RFPDK							
0x21	RW	CUS_RF10								
0x22	RW	CUS_RF11								
0x23	RW	CUS_RF12								
0x24	RW	CUS_FSK1								
0x25	RW	CUS_FSK2								
0x26	RW	CUS_FSK3								
0x27	RW	CUS_FSK4								
0x28	RW	CUS_FSK5								
0x29	RW	CUS_FSK6								
0x2A	RW	CUS_FSK7								
0x2B	RW	CUS_CDR1								
0x2C	RW	CUS_CDR2								
0x2D	RW	CUS_CDR3								
0x2E	RW	CUS_CDR4								
0x2F	RW	CUS_AGC1								
0x30	RW	CUS_AGC2								
0x31	RW	CUS_AGC3								
0x32	RW	CUS_AGC4								
0x33	RW	CUS_OOK1								
0x34	RW	CUS_OOK2								
0x35	RW	CUS_OOK3								
0x36	RW	CUS_OOK4								
0x37	RW	CUS_OOK5								

8.5 Baseband Bank

Baseband bank mainly stores the register with package setting.

Table 25. Baseband Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x38	RW	CUS_PKT1	RX_PREAM_SIZE [4:0]					PREAM_LENG_UNIT	DATA_MODE [1:0]	
0x39	RW	CUS_PKT2	TX_PREAM_SIZE [7:0]							
0x3A	RW	CUS_PKT3	TX_PREAM_SIZE [15:8]							
0x3B	RW	CUS_PKT4	PREAM_VALUE [7:0]							
0x3C	RW	CUS_PKT5	RESV	SYNC_TOL [2:0]			SYNC_SIZE [2:0]			SYNC_MAN_EN
0x3D	RW	CUS_PKT6	SYNC_VALUE [7:0]							
0x3E	RW	CUS_PKT7	SYNC_VALUE [15:8]							
0x3F	RW	CUS_PKT8	SYNC_VALUE [23:16]							
0x40	RW	CUS_PKT9	SYNC_VALUE [31:24]							
0x41	RW	CUS_PKT10	SYNC_VALUE [39:32]							
0x42	RW	CUS_PKT11	SYNC_VALUE [47:40]							
0x43	RW	CUS_PKT12								
0x44	RW	CUS_PKT13	SYNC_VALUE [63:56]							
0x45	RW	CUS_PKT14	RESV	PAYLOAD_LENG [10:8]			AUTO_ACK_EN	NODE_LENG_POS_SEL	PAYLOAD_BIT_ORDER	PKT_TYPE
0x46	RW	CUS_PKT15	PAYLOAD_LENG [7:0]							
0x47	RW	CUS_PKT16	RESV	RESV	NODE_FREE_EN	NODE_ERR_MASK	NODE_SIZE [1:0]		NODE_DET_MODE [1:0]	
0x48	RW	CUS_PKT17	NODE_VALUE [7:0]							
0x49	RW	CUS_PKT18	NODE_VALUE [15:8]							
0x4A	RW	CUS_PKT19	NODE_VALUE [23:16]							
0x4B	RW	CUS_PKT20	NODE_VALUE [31:24]							
0x4C	RW	CUS_PKT21	FEC_TYPE	FEC_EN	CRC_BYTE_SWAP	CRC_BIT_INV	CRC_RANGE	CRC_TYPE [1:0]		CRC_EN
0x4D	RW	CUS_PKT22	CRC_SEED [7:0]							
0x4E	RW	CUS_PKT23	CRC_SEED [15:8]							
0x4F	RW	CUS_PKT24	CRC_BIT_ORDER	WHITEN_SEED [8]	WHITEN_SEED_TYPE	WHITEN_TYPE [1:0]		WHITEN_EN	MANCH_TYPE	MANCH_EN
0x50	RW	CUS_PKT25	WHITEN_SEED [7:0]							
0x51	RW	CUS_PKT26	RESV	RESV	RESV	RESV	RESV	RESV	TX_PREFIX_TYPE [1:0]	
0x52	RW	CUS_PKT27	TX_PKT_NUM [7:0]							
0x53	RW	CUS_PKT28	TX_PKT_GAP [7:0]							
0x54	RW	CUS_PKT29	FIFO_AUTO_RES_EN	FIFO_TH [6:0]						

8.6 Tx Bank

Tx bank stores the register with transmit power, frequency offset.

Table 26. Tx Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x55	RW	CUS_TX1	User does not need to understand the detail, just directly export the register contents from the RFPDK							
0x56	RW	CUS_TX2								
0x57	RW	CUS_TX3								
0x58	RW	CUS_TX4								
0x59	RW	CUS_TX5								
0x5A	RW	CUS_TX6								
0x5B	RW	CUS_TX7								
0x5C	RW	CUS_TX8								
0x5D	RW	CUS_TX9								
0x5E	RW	CUS_TX10								
0x5F	RW	CUS_LBD								

8.7 Control Bank1

Control bank 1 stores the register with various functional modules enabling and function selection.

Table 27. Control Bank1

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	RW	CUS_MODE_CTL	CHIP_MODE_SWT [7:0]							
0x61	RW	CUS_MODE_STA	RESV	RESV	RSTN_IN_EN	CFG_RETAIN	CHIP_MODE_STA [3:0]			
0x62	RW	CUS_EN_CTL	RESV	RESV	UNLOCK_STOP_EN	LBD_STOP_EN	RESV	RESV	RESV	RESV
0x63	RW	CUS_FREQ_CHNL	FH_CHANNEL [7:0]							
0x64	RW	CUS_FREQ_OFS	FH_OFFSET [7:0]							
0x65	RW	CUS_IO_SEL	RESV	RESV	GPIO3_SEL [1:0]		GPIO2_SEL [1:0]		GPIO1_SEL [1:0]	
0x66	RW	CUS_INT1_CTL	RF_SWT1_EN	RF_SWT2_EN	INT_POLAR	INT1_SEL [4:0]				
0x67	RW	CUS_INT2_CTL	RESV	LFOSC_OUT_EN	TX_DIN_INV	INT2_SEL [4:0]				
0x68	RW	CUS_INT_EN	SL_TMO_EN	RX_TMO_EN	TX_DONE_EN	PREAM_OK_EN	SYNC_OK_EN	NODE_OK_EN	CRC_OK_EN	PKT_DONE_EN
0x69	RW	CUS_FIFO_CTL	TX_DIN_EN	TX_DIN_SEL [1:0]		FIFO_AUTO_CLR_DIS	FIFO_TX_RD_EN	FIFO_RX_TX_SEL	FIFO_MERGE_EN	SPI_FIFO_RD_WR_SEL
0x6A	W	CUS_INT_CLR1	RESV	RESV	SL_TMO_FLG	RX_TMO_FLG	TX_DONE_FLG	TX_DONE_CLR	SL_TMO_CLR	RX_TMO_CLR

8.8 Control Bank2

Control bank 2 stores the register with flag bit, RSSI and LBD. Note that the register cannot be accessed in the SLEEP state.

Table 28. Control Bank2

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x6B	W	**CUS_INT_CLR2**	RESV	RESV	LBD_CLR	PREAM_OK_CLR	SYNC_OK_CLR	NODE_OK_CLR	CRC_OK_CLR	PKT_DONE_CLR
0x6C	W	**CUS_FIFO_CLR**	RESV	RESV	RESV	RESV	RESV	FIFO_RESTORE	FIFO_CLR_RX	FIFO_CLR_TX
0x6D	R	**CUS_INT_FLAG**	LBD_FLG	COL_ERR_FLG	PKT_ERR_FLG	PREAM_OK_FLG	SYNC_OK_FLG	NODE_OK_FLG	CRC_OK_FLG	PKT_OK_FLG
0x6E	R	**CUS_FIFO_FLAG**	RESV	RX_FIFO_FULL_FLG	RX_FIFO_NMTY_FLG	RX_FIFO_TH_FLG	RX_FIFO_OVF_FLG	TX_FIFO_FULL_FLG	TX_FIFO_NMTY_FLG	TX_FIFO_TH_FLG
0x6F	R	**CUS_RSSI_CODE**	RSSI_CODE [7:0]							
0x70	R	**CUS_RSSI_DBM**	RSSI_DBM [7:0]							
0x71	R	**CUS_LBD_RESULT**	LBD_RESULT [7:0]							

9. Ordering Information

Table 29. CMT2300A ordering information

Part Number	Descriptions	Packaging	Packing	Condition	MOQ
CMT2300A-EQR[1]	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver	QFN16 (3x3)	Tape & Reel	1.8 to 3.6V, -40 to 85℃	5,000

Note:

[1]. "E" represents extended industrial grade. The temperature range is from -40 to +85.
"Q" represents QFN16 packaging.
"R" represents tape & reel packing. MOQ is 5000 pcs.

For more information about product, please visit www.cmostek.com.
For purchasing or price requirements, please contact sales@cmostek.com or local sales representative.

10. Packaging Information

CMT2300A packaging is QFN16 (3x3). The packaging information is as below.

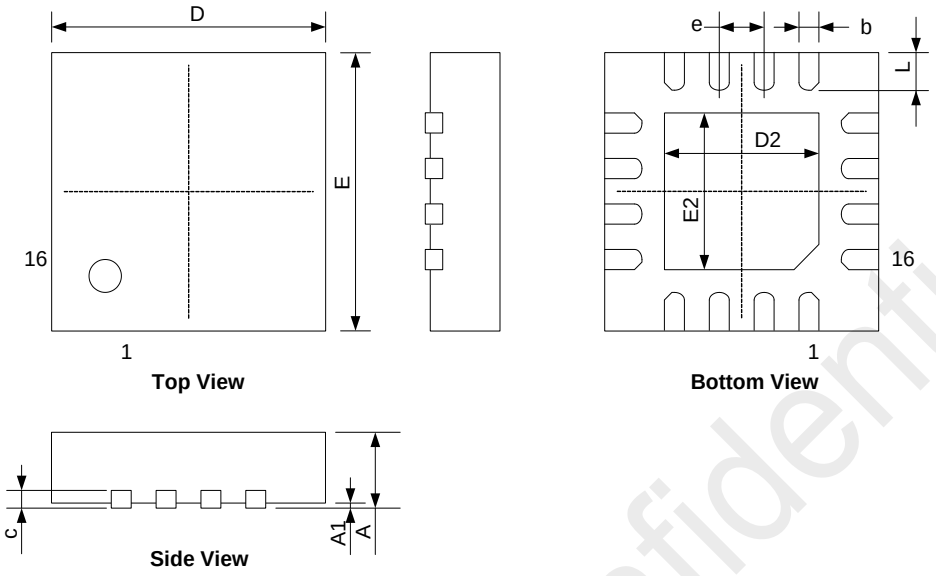


Figure 21. 16-Pin QFN 3x3 packaging

Table 30. 16-Pin QFN 3x3 Packaging Size

Symbol	Size (mm)	
	Min.	Max.
A	0.7	0.8
A1	—	0.05
b	0.18	0.30
c	0.18	0.25
D	2.90	3.10
D2	1.55	1.75
e	0.50 BSC	
E	2.90	3.10
E2	1.55	1.75
L	0.35	0.45

11. Top Marking

11.1 CMT2300A Top Marking

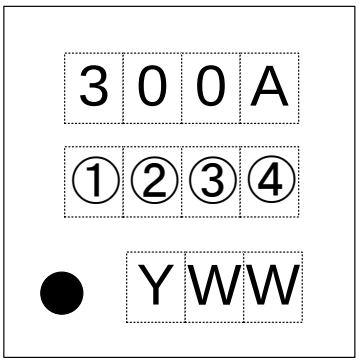


Figure 22. CMT2300A top marking

Table 31. CMT2300A top marking description

Marking method	Laser
Pin 1 mark	Circle diameter = 0.3 mm
Font size	0.5 mm, right aligned.
Line 1 marking	300A represents model CMT2300A
Line 2 marking	①②③④ **represents th**e internal tracking coding
Line 3 marking	Date code is assigned by assembly factory. Y represents the last digit of the year. WW represents working week.

12. Other Documentations

Table 32. CMT2300A related documents

Doc. No.	Doc. Name	Descriptions
AN141	CMT2300A Schematic and PCB Layout Design Guideline	Introduces CMT2300A PCB schematic and layout design rules, RF matching network and other layout considerations.

13. Document Change List

Table 33. Document Change List

Rev. No.	Chapter	Change Descriptions	Date
Preliminary	All	Preliminary version for internal verification	2015-06-09
Preliminary 0.2	5.14.1 5.14.2	Update 1st paragraph Update Table 34	2015-06-10
0.6	All	Split Chapter 5 and 6 from Chapter 4	2015-08-06
0.7	All	Initial release for production version	2017-03-22

14. Contact Information

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